

WHAT IS CLAIMED IS:

1 1. A computer program product comprising instructions which are stored in a
2 memory and which, upon execution by a processor, perform steps of:
3 generating an admittance matrix for an electrical circuit which is being analyzed,
4 the admittance matrix including symbolic expressions rather than numerical
5 expressions for at least some components of the electrical circuit;
6 linearly and algebraically solving an equation system including the admittance
7 matrix for analyzing at least a part of the electrical circuit.

1 2. The computer program product of claim 1, further comprising linearly and
2 algebraically solving the equation system including the admittance matrix for one of (1)
3 determining a transfer function between specified nodes of the electrical circuit; (2)
4 optimizing a component of the electrical circuit; (3) perturbation/sensitivity analysis,
5 and (4) general circuit design..

1 3. The computer program product of claim 1, wherein the electrical circuit has a
2 telecommunications component including one of a multi-winded transformer, a loading
3 coil, a line-driver, an analogue cable, and a filter.

1 4. The computer program product of claim 1, wherein the admittance matrix
2 comprises admittance blocks for each of plural subcircuits.

1 5. The computer program product of claim 4, wherein the admittance blocks for
2 the plural subcircuits are situated on a main diagonal of the admittance matrix, and
3 wherein connectivity blocks which represent connectivity between the plural
4 subcircuits are situated symmetrically across the main diagonal of the admittance
5 matrix.

1 6. The computer program product of claim 1, further comprising
2 (a) rearranging equations in the equation system in accordance with an
3 identification of interesting nodes for analysis;
4 (b) partitioning the admittance matrix into partitions accordance with the
5 identification of interesting nodes for analysis;
6 (c) generating a simplified equation system based on the partitioning of step (b).

1 7. The computer program product of claim 6, further comprising as step (b)
2 recursively partitioning the admittance matrix into partitions accordance with the
3 identification of interesting nodes for analysis.

1 8. A computer program product comprising instructions which are stored in a
2 memory and which, upon execution by a processor, perform steps of:
3 generating an admittance matrix for an electrical circuit which is being analyzed,
4 the admittance matrix including symbolic expressions rather than numerical
5 expressions for at least some components of the electrical circuit;
6 using symbolic computation to solve an equation system including the
7 admittance matrix for analyzing at least a part of the electrical circuit.

1 9. The computer program product of claim 8, further comprising using symbolic
2 computation to solve an equation system for one of (1) determining a transfer function
3 between specified nodes of the electrical circuit; (2) optimizing a component of the
4 electrical circuit; (3) perturbation/sensitivity analysis, and (4) general circuit design.

1 10. The computer program product of claim 9, wherein the electrical circuit has
2 a telecommunications component including one of a multi-winded transformer, a
3 loading coil, a line-driver, an analogue cable, and a filter.

1 11. The computer program product of claim 9, wherein the admittance matrix
2 comprises admittance blocks for each of plural subcircuits.

1 12. The computer program product of claim 11, wherein the admittance blocks
2 for the plural subcircuits are situated on a main diagonal of the admittance matrix, and
3 wherein connectivity blocks which represent connectivity between the plural
4 subcircuits are situated symmetrically across the main diagonal of the admittance
5 matrix.

1 13. The computer program product of claim 8, further comprising
2 a) rearranging equations in the equation system in accordance with an
3 identification of interesting nodes for analysis;
4 (b) partitioning the admittance matrix into partitions accordance with the
5 identification of interesting nodes for analysis;

6 (c) generating a simplified equation system based on the partitioning of step (b).

1 14. The computer program product of claim 13, further comprising as step (b)
2 recursively partitioning the admittance matrix into partitions accordance with the
3 identification of interesting nodes for analysis.

1 15. A computer program product comprising instructions which are stored in a
2 memory and which, upon execution by a processor, perform steps of:
3 generating an admittance matrix for an electrical circuit which is being analyzed
4 by:

5 generating a main circuit admittance block for a main circuit comprising
6 the electrical circuit which is being analyzed;

7 generating a subcircuit admittance block for a subcircuit comprising the
8 electrical circuit which is being analyzed;

9 inserting the main circuit admittance block and the subcircuit admittance
10 block on a main diagonal of the admittance matrix;

11 generating connectivity blocks which represent connectivity between the
12 main circuit and the subcircuit;

13 inserting the connectivity blocks symmetrically across the main diagonal
14 of the admittance matrix;

15 using the admittance matrix for analyzing at least a part of the electrical circuit.

1 16. The computer program product of claim 15, wherein the step of generating
2 the subcircuit admittance block for the subcircuit comprises:

3 generating a subblock for the subcircuit;

4 generating an internal voltage subblock for the subcircuit; and

5 generating a surface connectivity subblock for the subcircuit.

1 17. The computer program product of claim 15, wherein the step of generating
2 the subblock for the subcircuit comprises generating one of an impedance subblock, a
3 chain matrix equation, and a scattering matrix.

1 18. The computer program product of claim 15, wherein the step of generating
2 connectivity blocks comprises:

3 generating a current exchange connectivity block which describes how currents
4 are exchanged between the main circuit and the subcircuit;

5 generating a voltage potential connectivity block which describes voltages at
6 common nodes between the main circuit and the subcircuit;

7 inserting the current exchange connectivity block and the voltage potential
8 connectivity block in the admittance matrix.

1 19. The computer program product of claim 15, further comprising using the
2 admittance matrix for one of (1) determining a transfer function between specified
3 nodes of the electrical circuit; (2) optimizing a component of the electrical circuit; (3)
4 perturbation/sensitivity analysis, and (4) general circuit design.

1 20. The computer program product of claim 15, wherein the subcircuit
2 comprises one of a multi-winded transformer, a loading coil, a line-driver, an analogue
3 cable, and a filter.

1 21. A method of analyzing an electric circuit comprising:
2 using a computer to generate an admittance matrix for the electrical circuit, the
3 admittance matrix including symbolic expressions rather than numerical expressions for
4 at least some components of the electrical circuit;
5 using the computer to linearly and algebraically solve an equation system
6 including the admittance matrix for analyzing at least a part of the electrical circuit.

1 22. The method of claim 21, further comprising linearly and algebraically
2 solving the equation system including the admittance matrix for one of (1) determining
3 a transfer function between specified nodes of the electrical circuit; (2) optimizing a
4 component of the electrical circuit; (3) perturbation/sensitivity analysis, and (4) general
5 circuit design.

1 23. The method of claim 21, wherein the electrical circuit has a
2 telecommunications component including one of a multi-winded transformer, a loading
3 coil, a line-driver, an analogue cable, and a filter.

1 24. The method of claim 21, wherein the admittance matrix comprises
2 admittance blocks for each of plural subcircuits.

1 25. The method claim 21, further comprising situating the admittance blocks for
2 the plural subcircuits on a main diagonal of the admittance matrix, and situating
3 connectivity blocks which represent connectivity between the plural subcircuits
4 symmetrically across the main diagonal of the admittance matrix.

1 26. The method claim 21, further comprising:

1 (a) rearranging equations in the equation system in accordance with an
2 identification of interesting nodes for analysis;

3 (b) partitioning the admittance matrix into partitions accordance with the
4 identification of interesting nodes for analysis;

5 (c) generating a simplified equation system based on the partitioning of step (b).

6 (d) solving the simplified equation system.

1 27. The method claim 26, further comprising as step (b) recursively partitioning
2 the admittance matrix into partitions in accordance with the identification of interesting
3 nodes for analysis.

1 28. A method of analyzing an electric circuit comprising:

2 using a computer to generate an admittance matrix for the electrical circuit, the
3 admittance matrix including symbolic expressions rather than numerical expressions for
4 at least some components of the electrical circuit;

5 using symbolic computation performed by the computer to solve an equation
6 system including the admittance matrix for analyzing at least a part of the electrical
7 circuit.

1 29. The method of claim 28, further comprising using the symbolic computation
2 to solve the equation system for one of (1) determining a transfer function between
3 specified nodes of the electrical circuit; (2) optimizing a component of the electrical
4 circuit; (3) perturbation/sensitivity analysis, and (4) general circuit design.

1 30. The method of claim 28, wherein the electrical circuit has a
2 telecommunications component including one of a multi-winded transformer, a loading
3 coil, a line-driver, an analogue cable, and a filter.

1 31. The method of claim 28, wherein the admittance matrix comprises
2 admittance blocks for each of plural subcircuits.

1 32. The method of claim 28, comprising situating the admittance blocks for the
2 plural subcircuits on a main diagonal of the admittance matrix, and situating
3 connectivity blocks which represent connectivity between the plural subcircuits
4 symmetrically across the main diagonal of the admittance matrix.

1 33. The method claim 28, further comprising:

1 (a) rearranging equations in the equation system in accordance with an
2 identification of interesting nodes for analysis;

3 (b) partitioning the admittance matrix into partitions accordance with the
4 identification of interesting nodes for analysis;

5 (c) generating a simplified equation system based on the partitioning of step (b).

1 34. The method of claim 33, further comprising as step (b) recursively
2 partitioning the admittance matrix into partitions in accordance with the identification
3 of interesting nodes for analysis.

1 35. A method of analyzing an electric circuit comprising:

2 using a computer to generate an admittance matrix for the electrical circuit by:

3 generating a main circuit admittance block for a main circuit comprising
4 the electrical circuit which is being analyzed;

5 generating a subcircuit admittance block for a subcircuit comprising the
6 electrical circuit which is being analyzed;

7 inserting the main circuit admittance block and the subcircuit admittance
8 block on a main diagonal of the admittance matrix;

9 generating connectivity blocks which represent connectivity between the
10 main circuit and the subcircuit;

11 inserting the connectivity blocks symmetrically across the main diagonal
12 of the admittance matrix;

13 using the admittance matrix for analyzing at least a part of the electrical circuit.

1 36. The method of claim 35, wherein generating the subcircuit admittance block
2 for the subcircuit comprises:

3 generating a subblock for the subcircuit;
4 generating an internal voltage subblock for the subcircuit; and
5 generating a surface connectivity subblock for the subcircuit.

1 37. The method of claim 35, wherein the step of generating the subblock for the
2 subcircuit comprises generating one of an impedance subblock, a chain matrix
3 equation, and a scattering matrix.

1 38. The method of claim 35, wherein the step of generating connectivity blocks
2 comprises:

3 generating a current exchange connectivity block which describes how currents
4 are exchanged between the main circuit and the subcircuit;

5 generating a voltage potential connectivity block which describes voltages at
6 common nodes between the main circuit and the subcircuit;

7 inserting the current exchange connectivity block and the voltage potential
8 connectivity block in the admittance matrix.

1 39. The method of claim 35, further comprising using the admittance
2 matrix for one of (1) determining a transfer function between specified nodes of the
3 electrical circuit; (2) optimizing a component of the electrical circuit; (3)
4 perturbation/sensitivity analysis, and (4) general circuit design.

1 40. The method of claim 35, wherein the subcircuit comprises one of a
2 multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter.